

FIG. 4

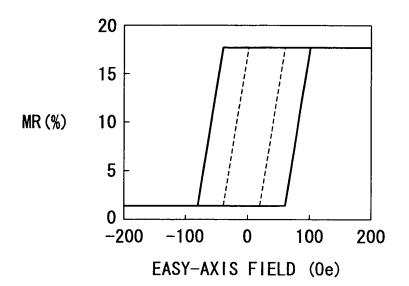
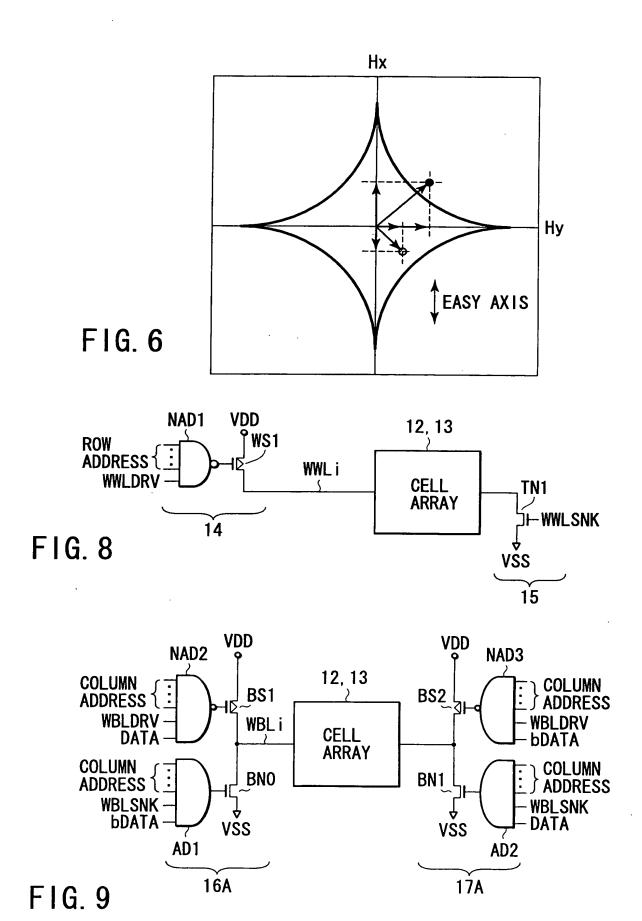
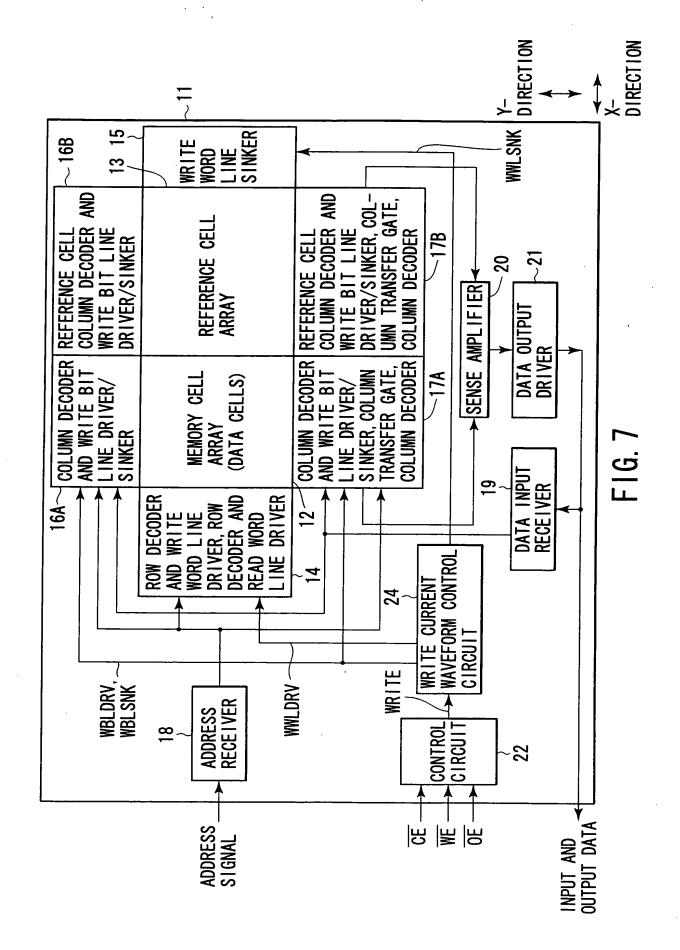


FIG. 5





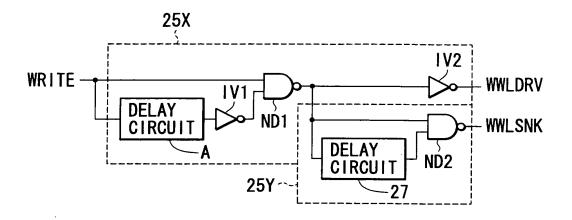


FIG. 10

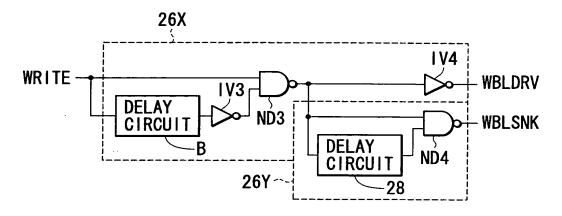


FIG. 11

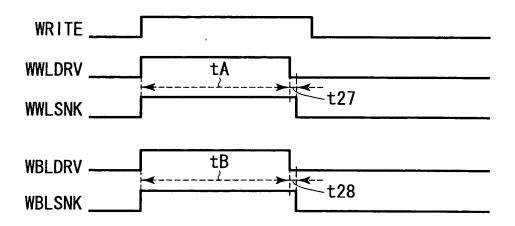
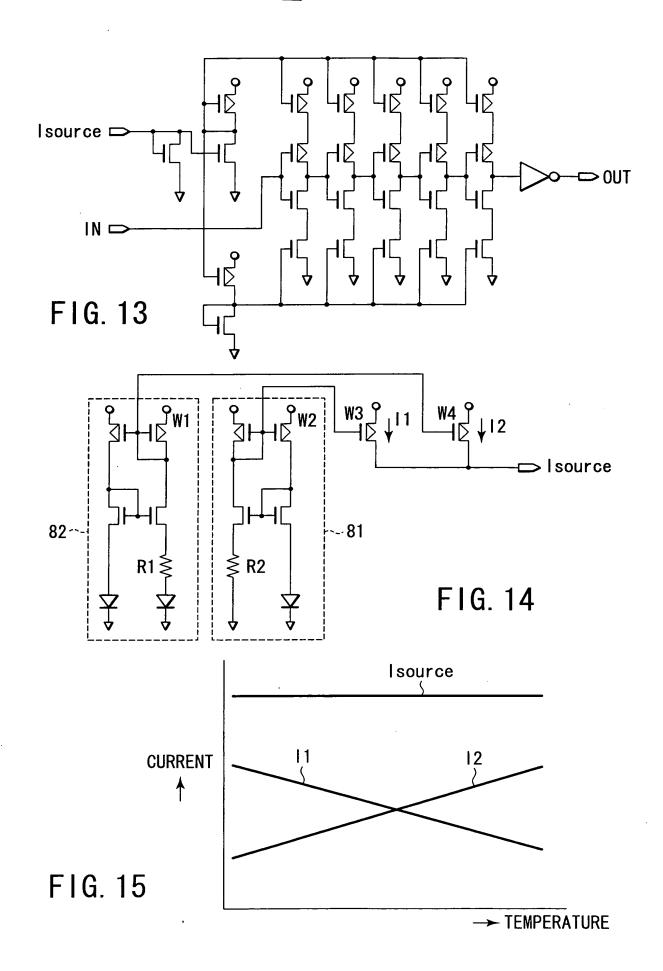


FIG. 12



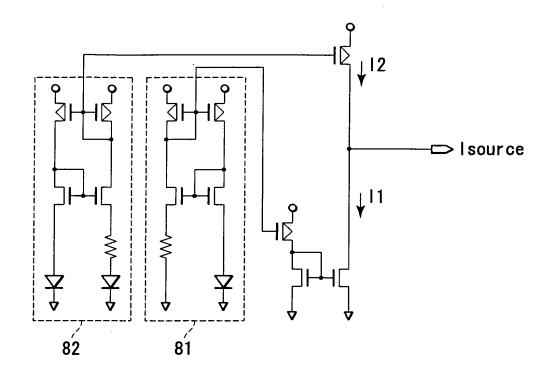


FIG. 16

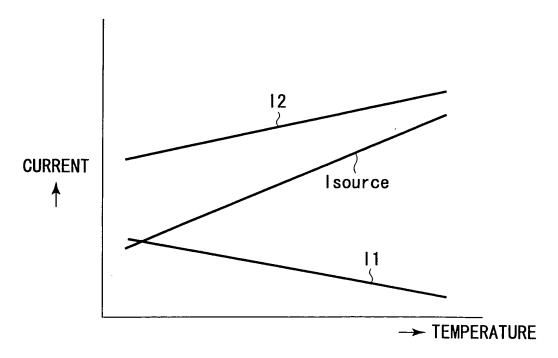


FIG. 17

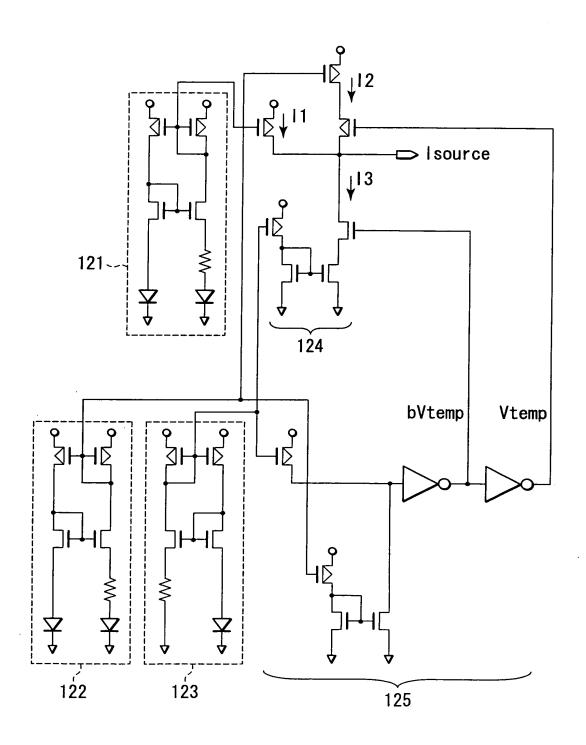
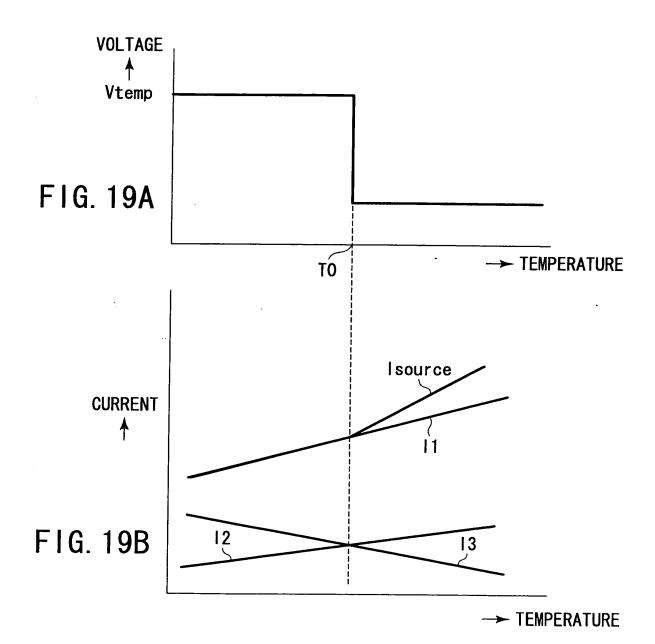


FIG. 18



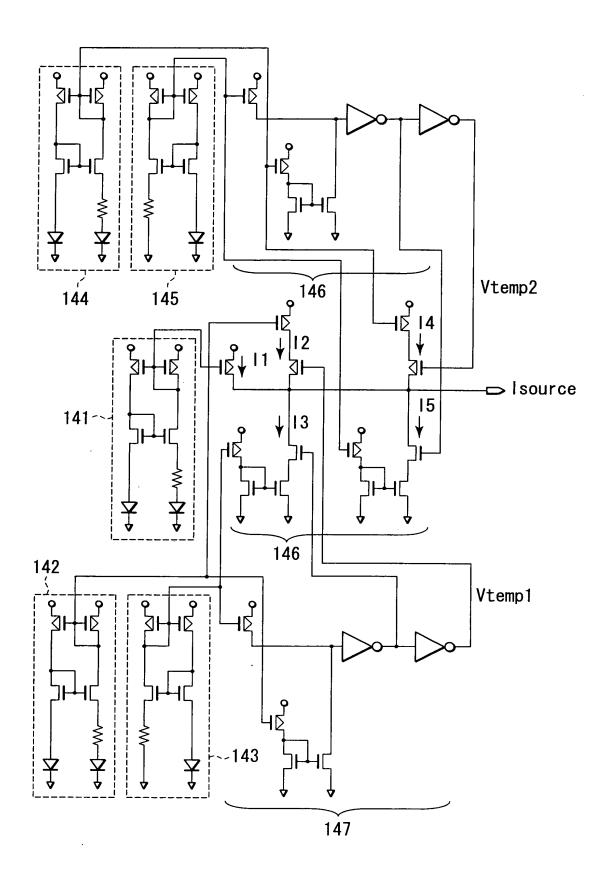
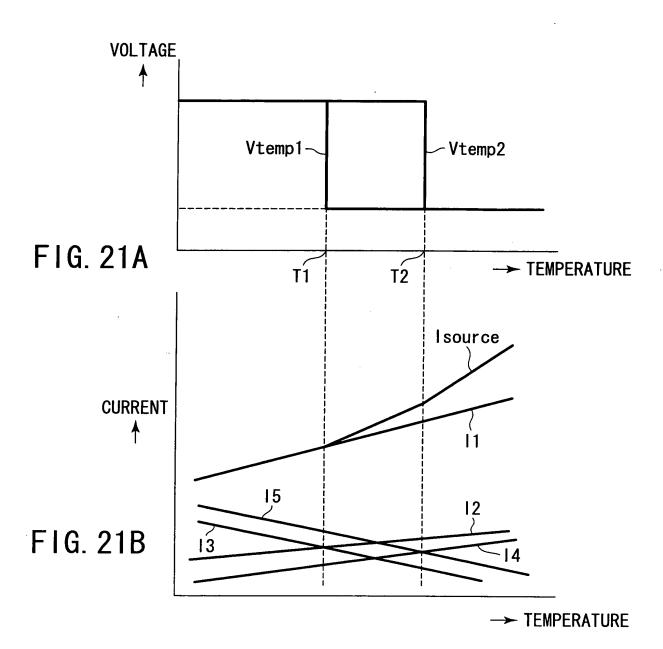
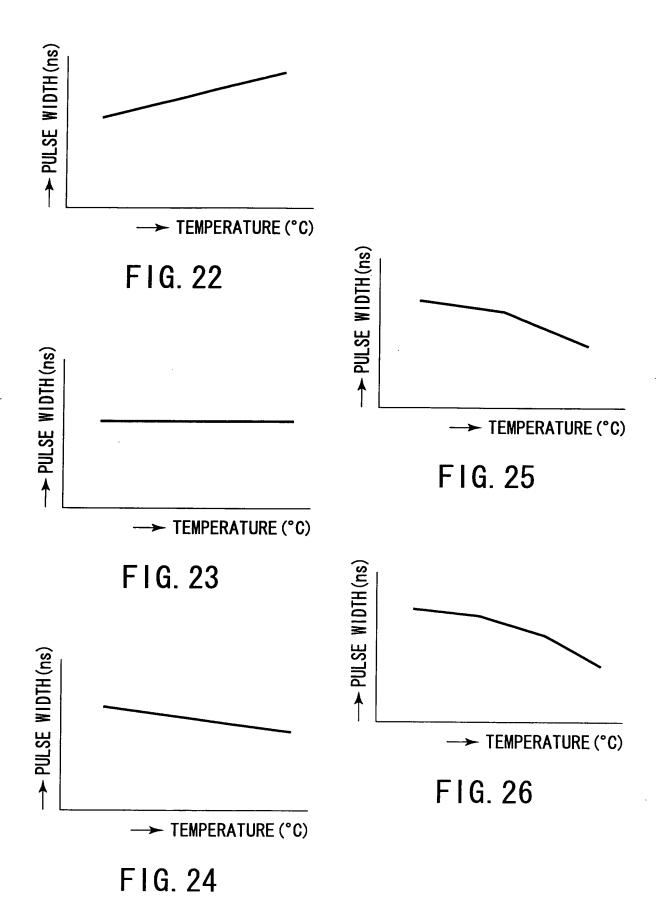


FIG. 20



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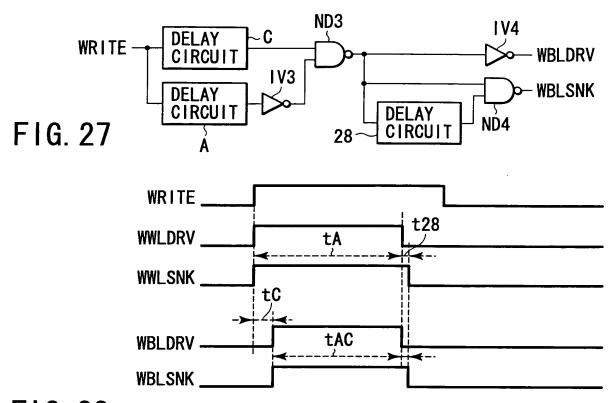
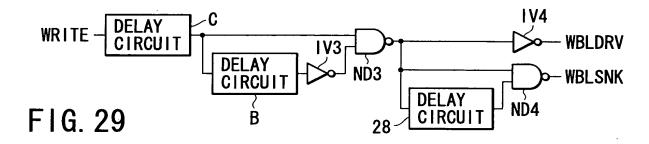


FIG. 28



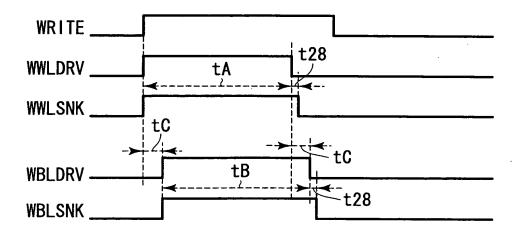
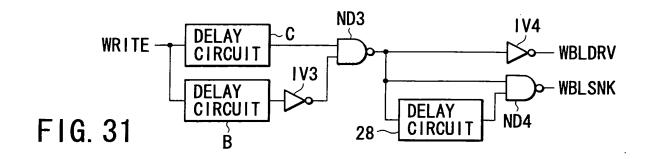


FIG. 30



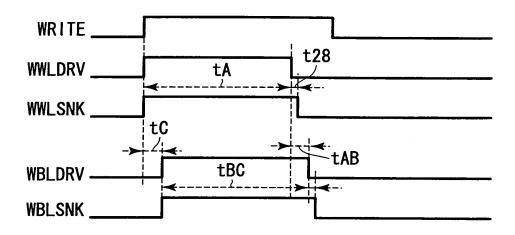


FIG. 32

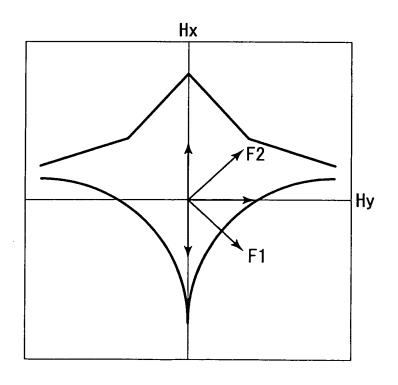


FIG. 33

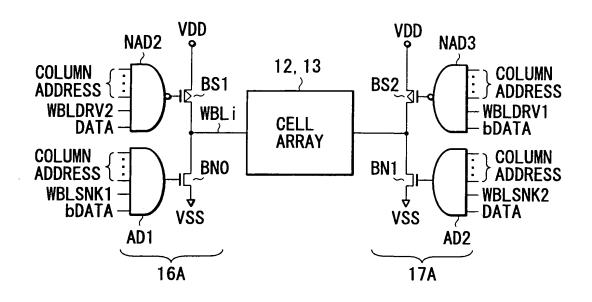
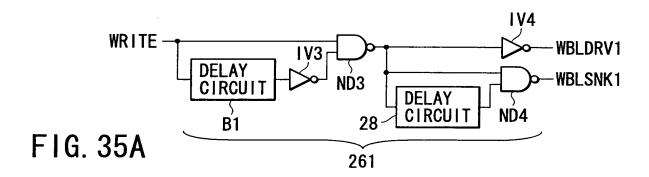
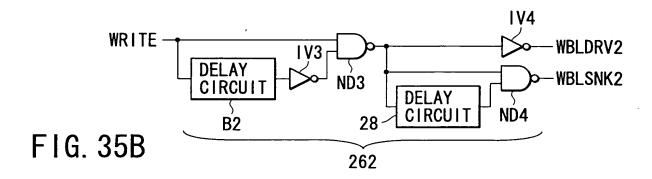


FIG. 34





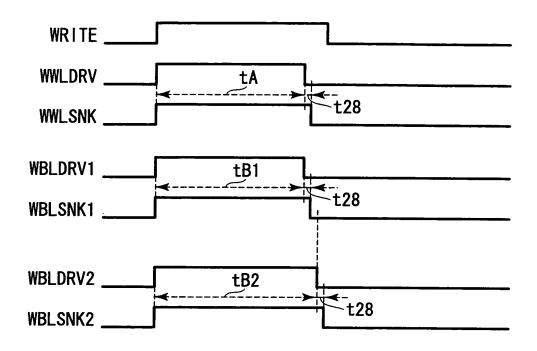


FIG. 36

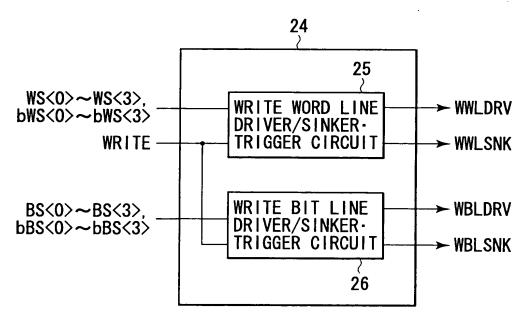
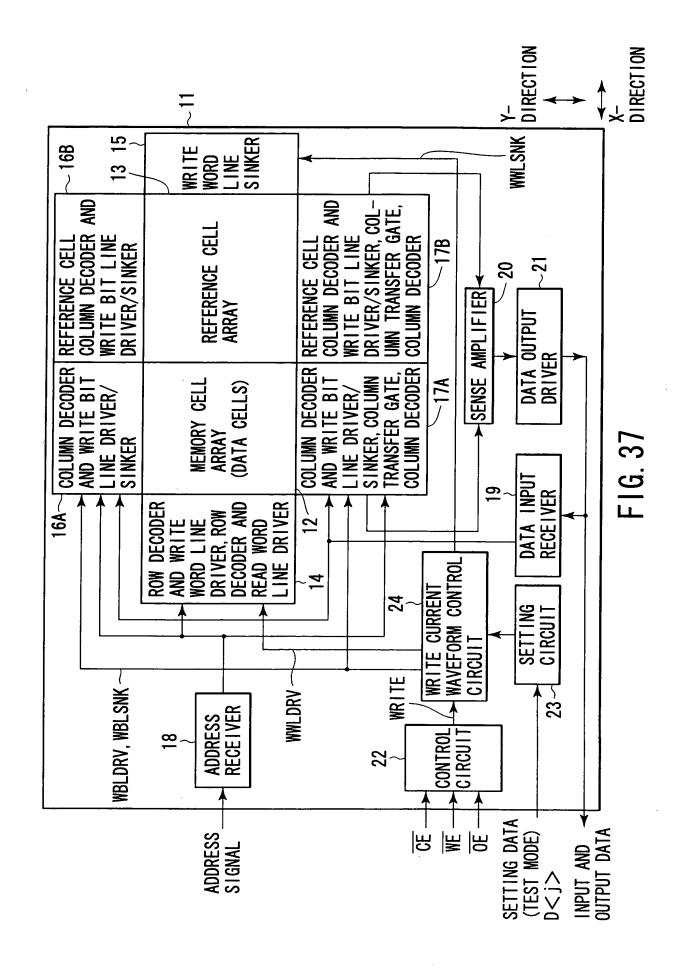
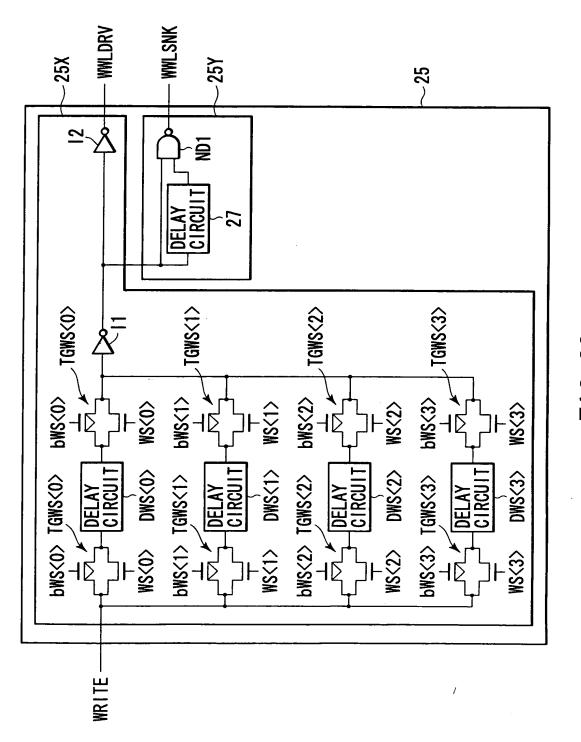
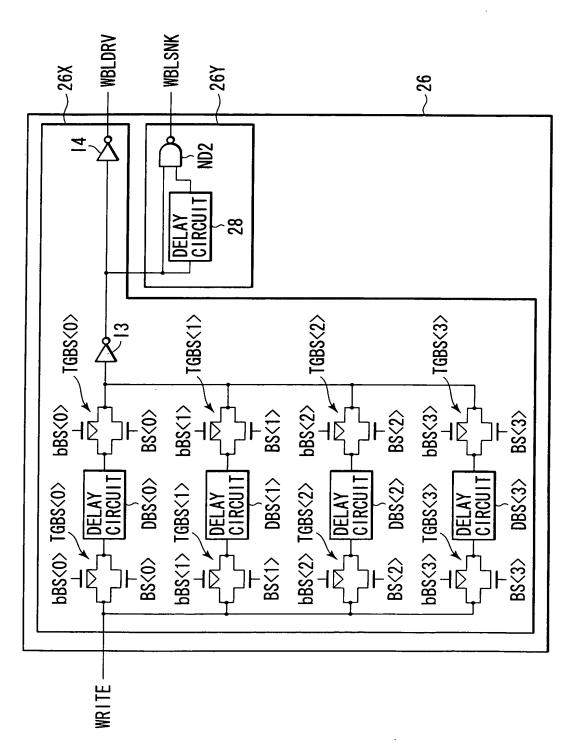


FIG. 38

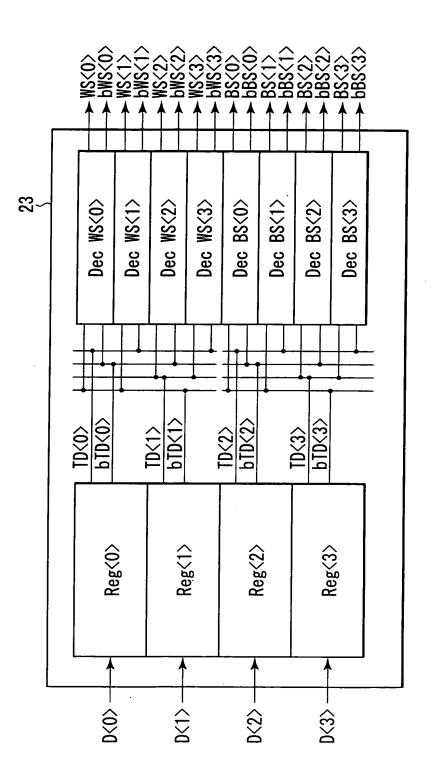




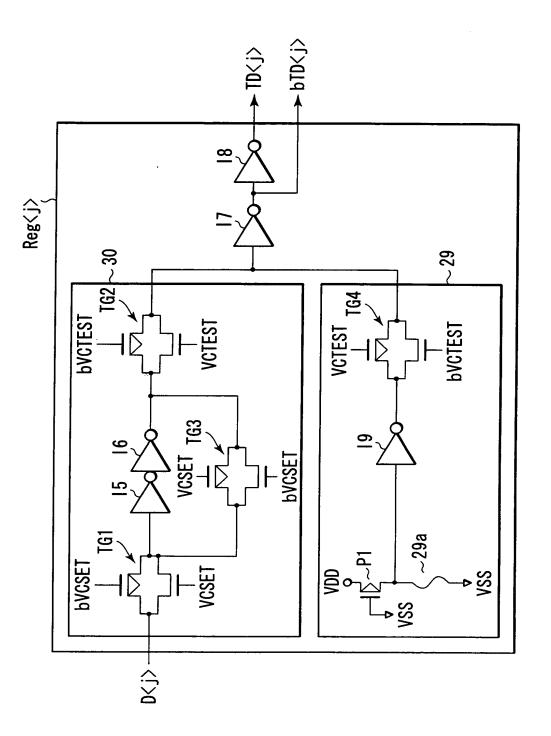
F1G. 39



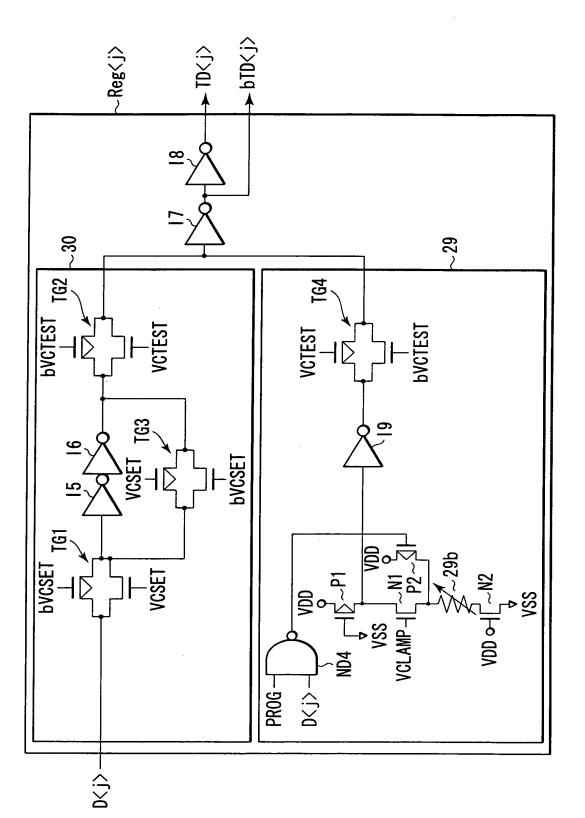
F1G. 40



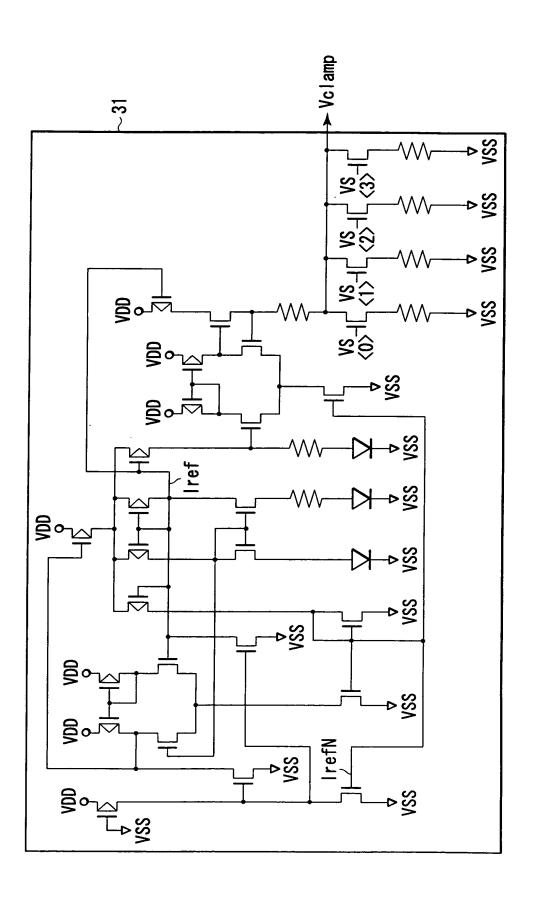
F1G. 41



F1G. 42

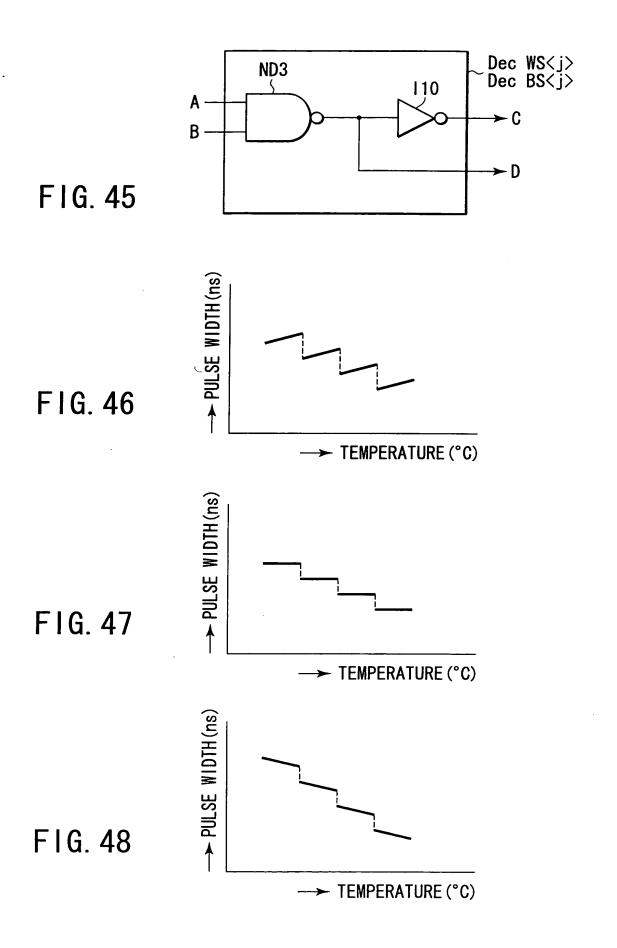


F1G. 43



F1G. 44

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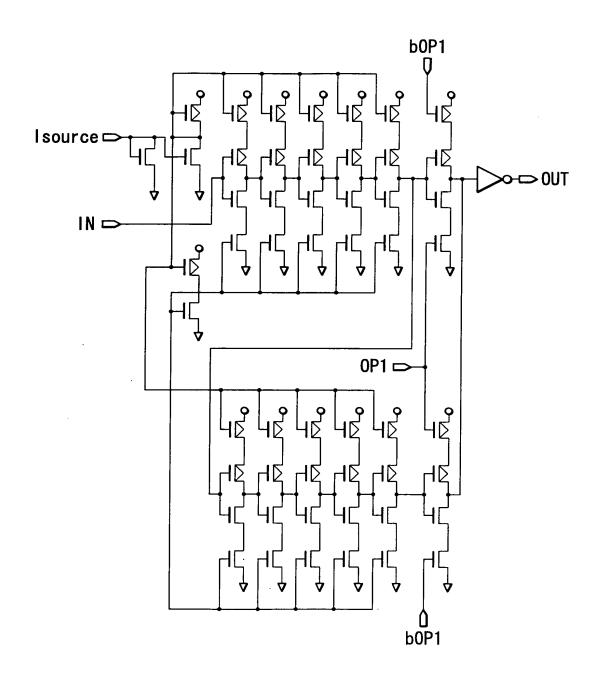


FIG. 49

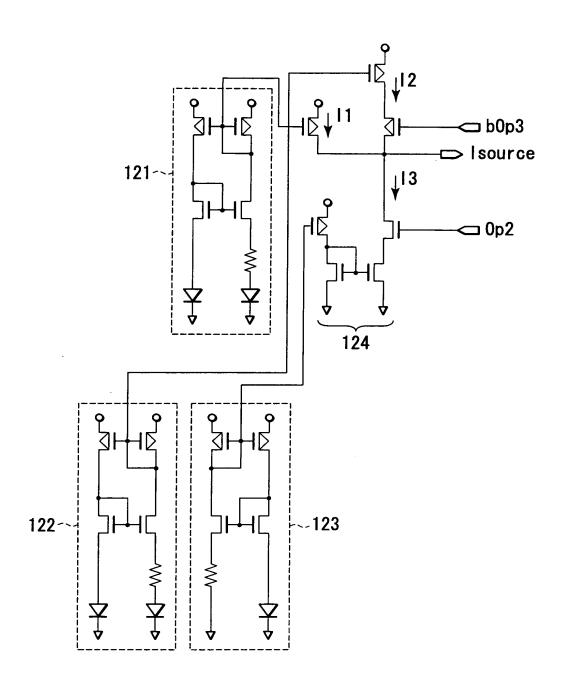
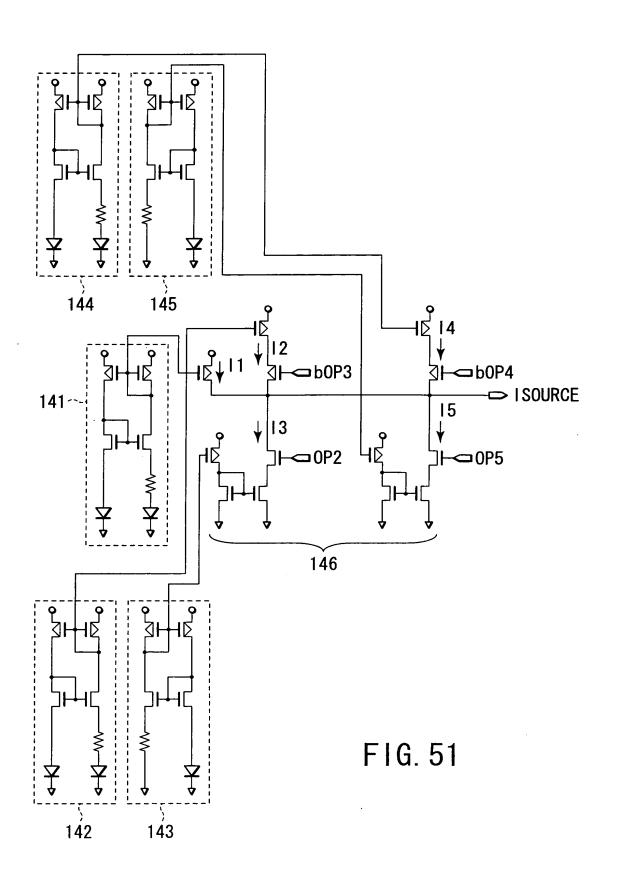
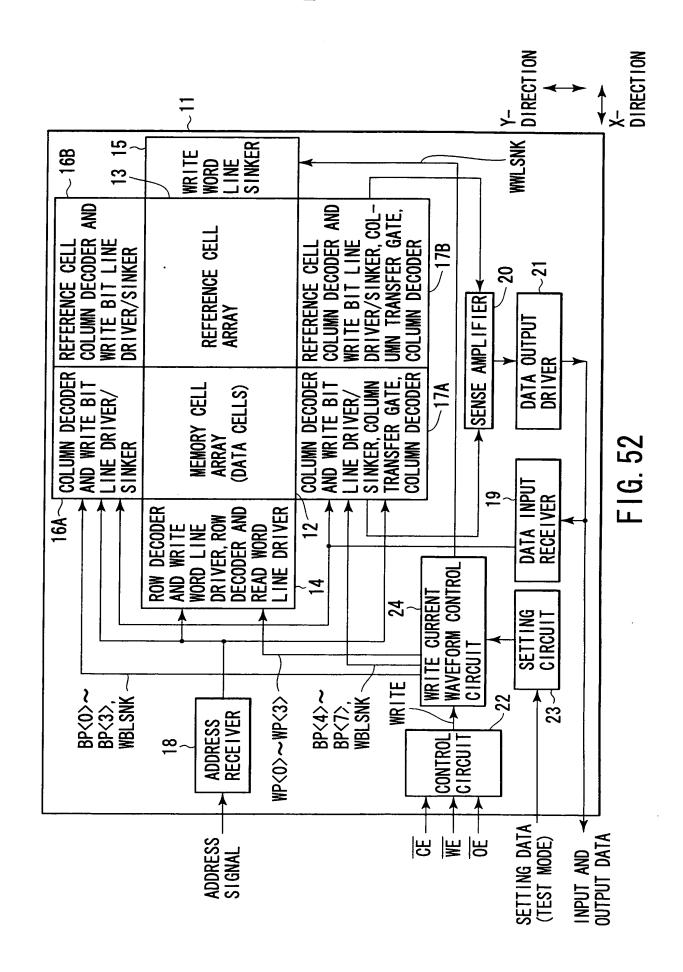
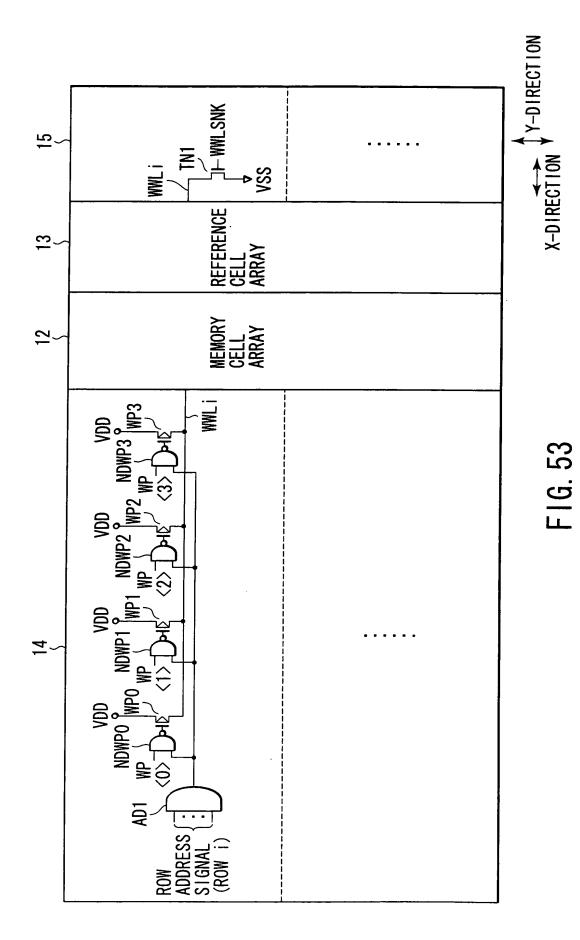


FIG. 50







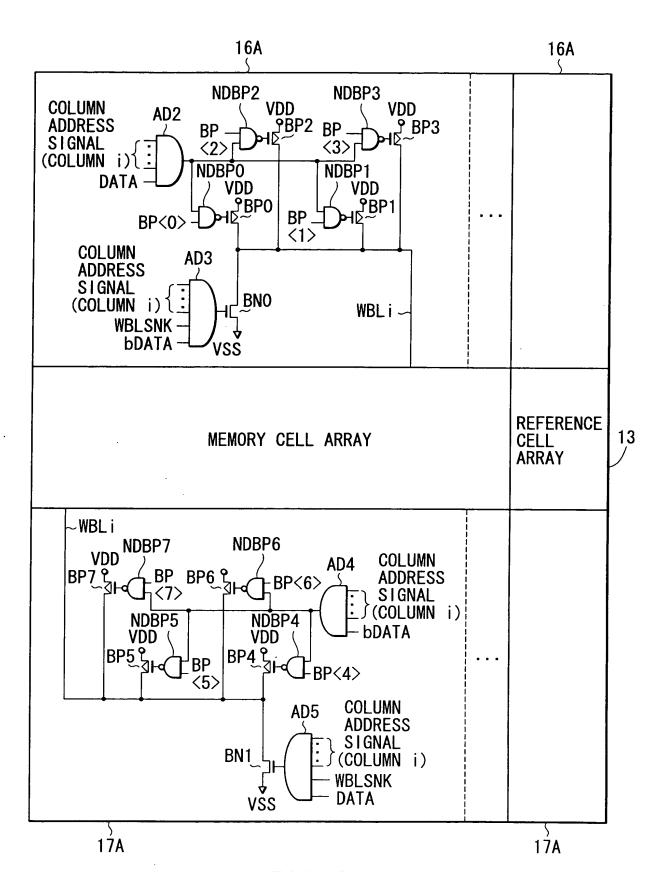


FIG. 54

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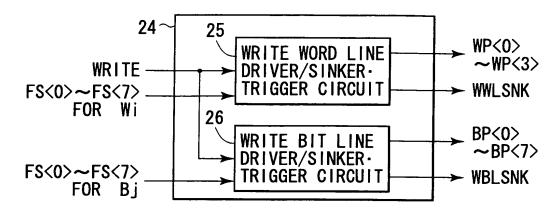


FIG. 55

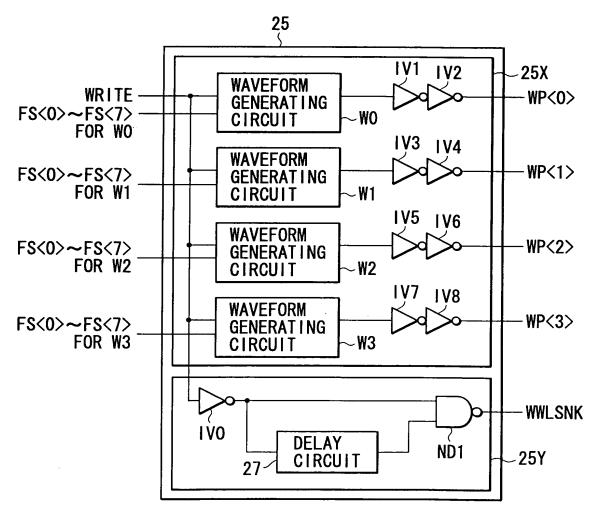


FIG. 56

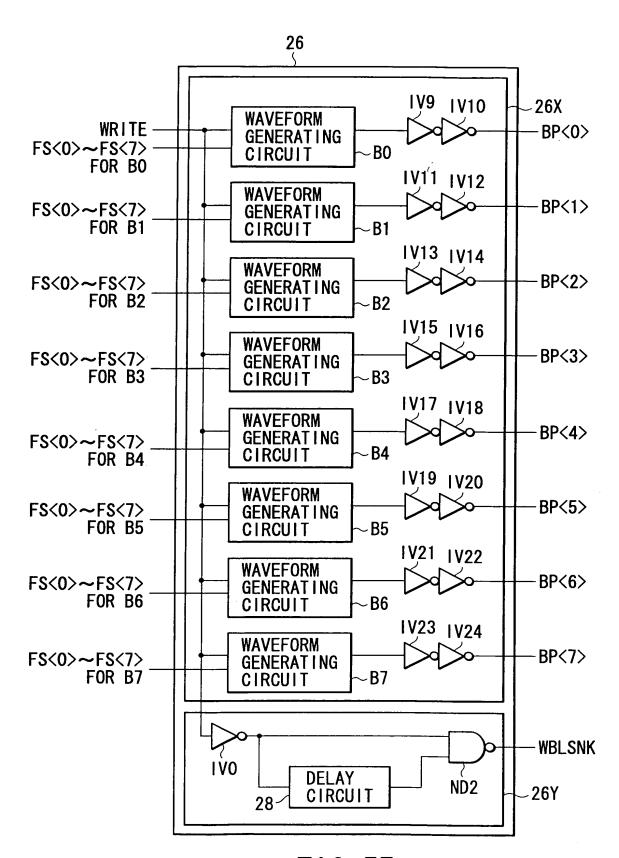
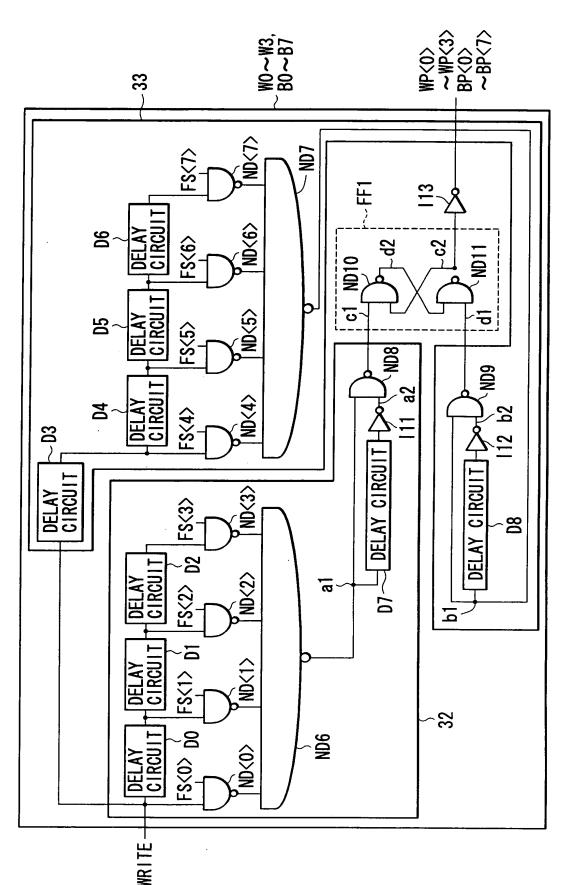


FIG. 57



F1G. 58

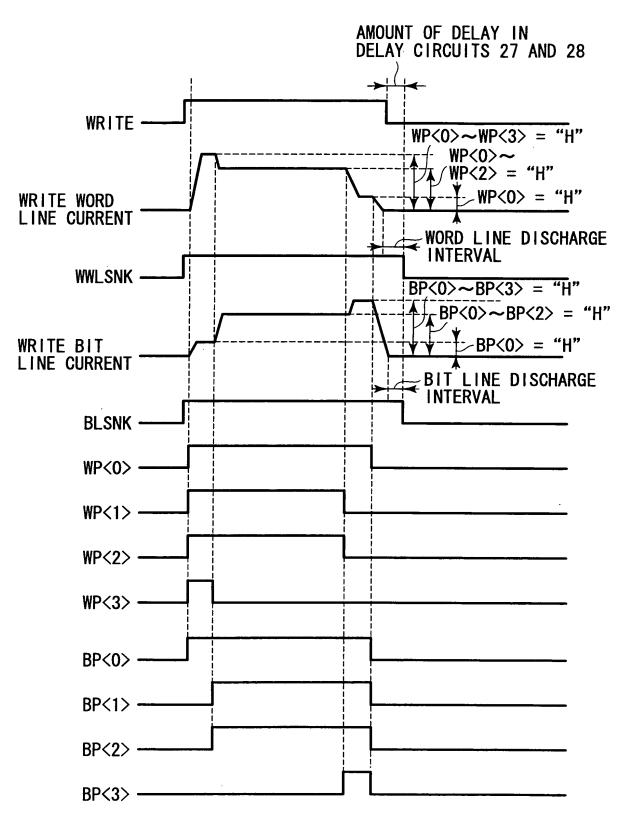
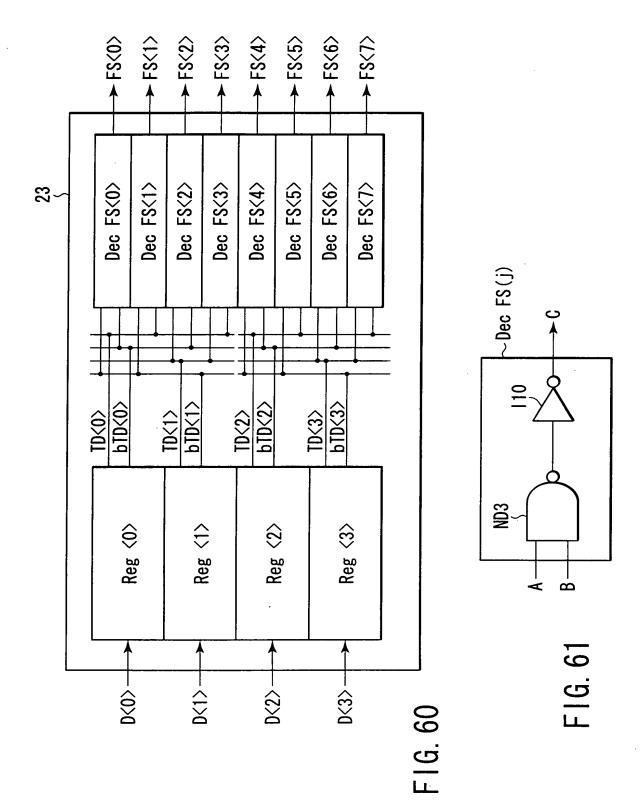
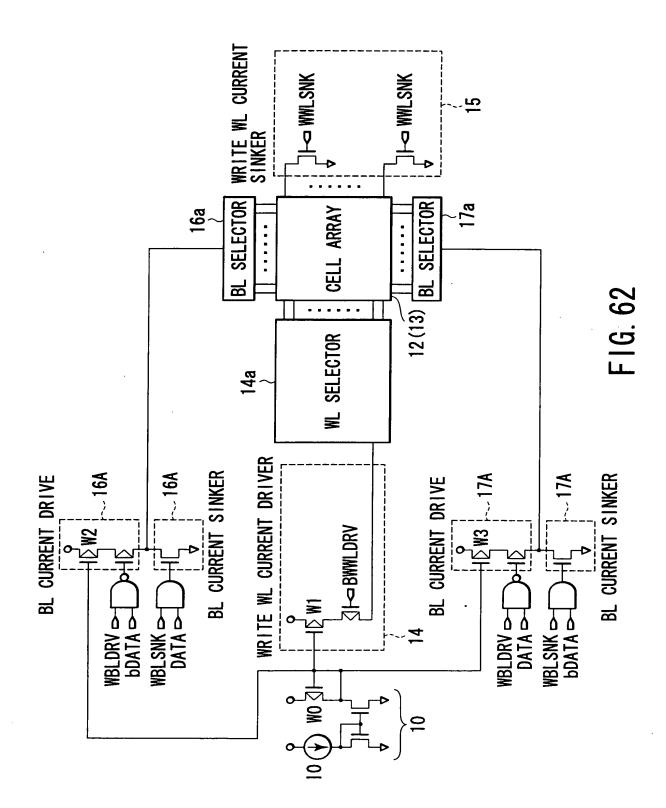


FIG. 59





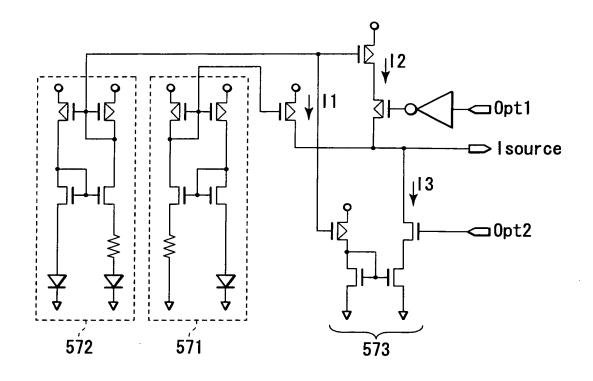


FIG. 63

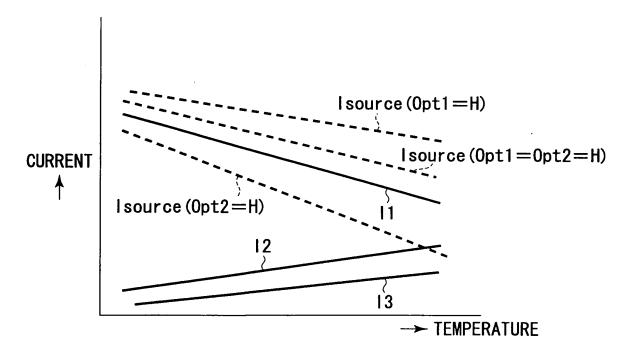


FIG. 64

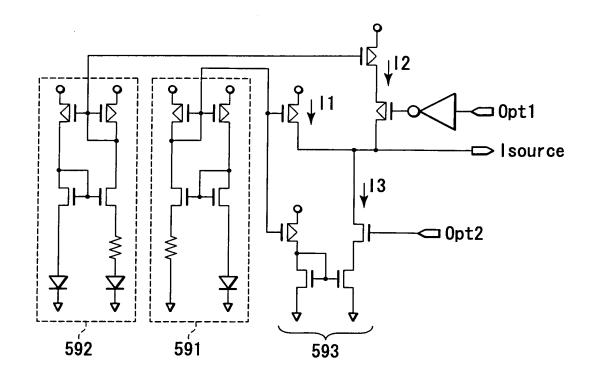


FIG. 65

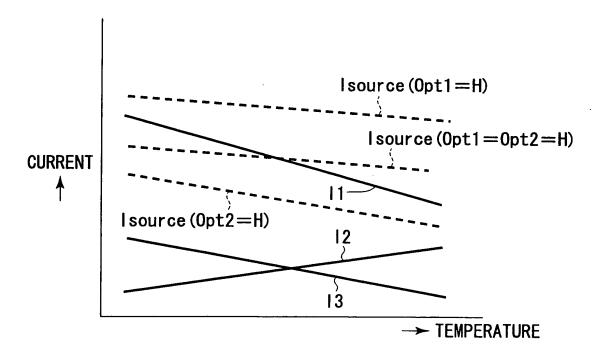
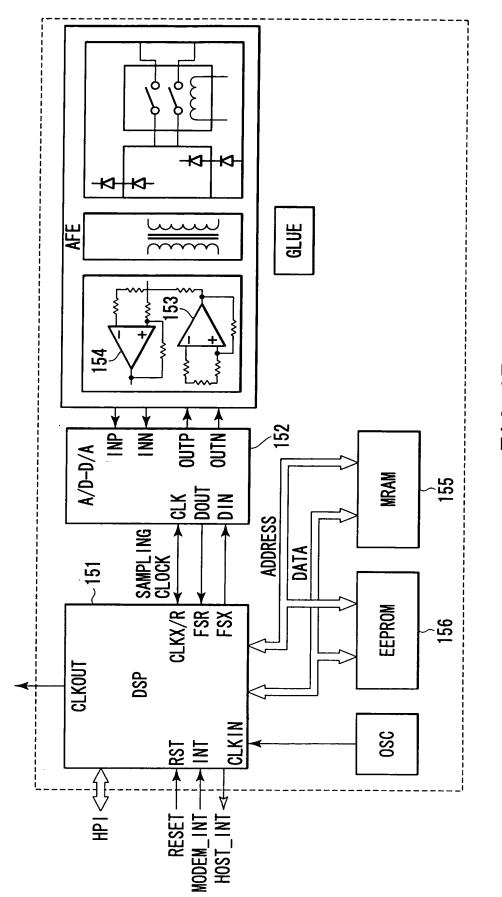
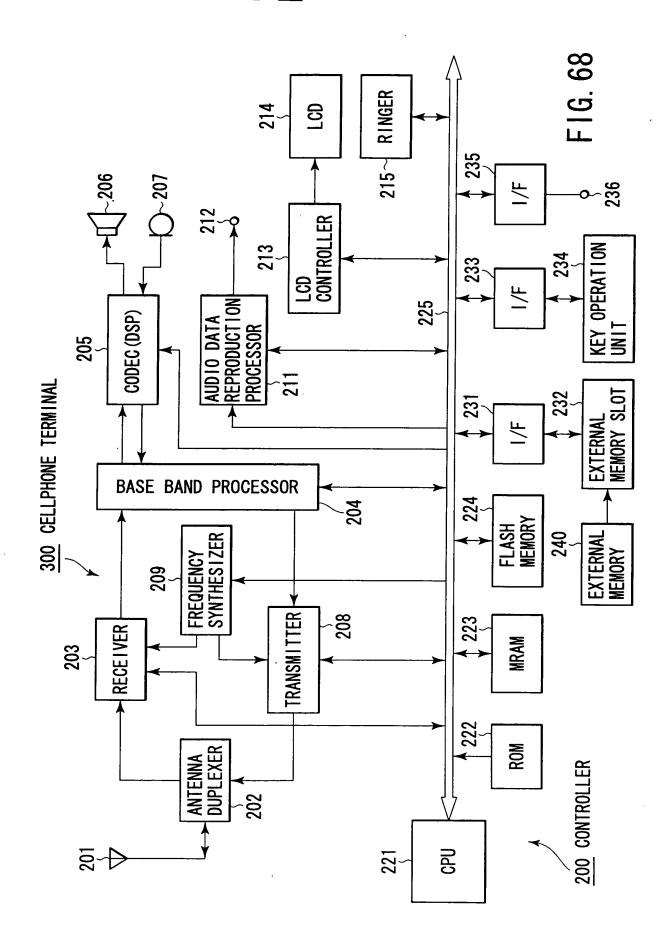
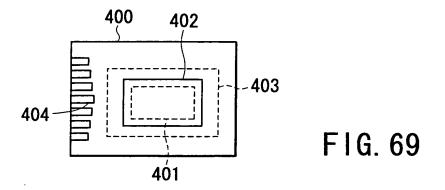


FIG. 66



F1G. 67





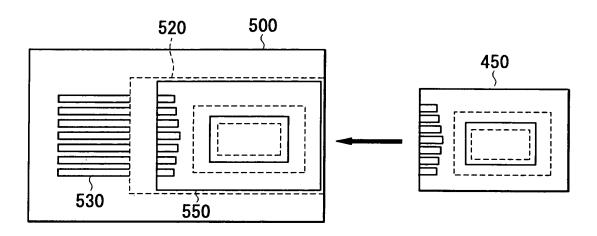
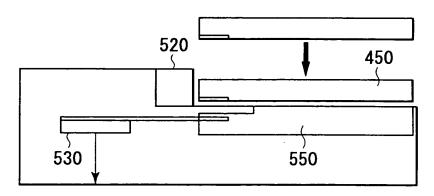


FIG. 70



TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 72

